KASUS 2 RANGKAIAN SEKUENSIAL

Deskripsi :

Pada Kasus Teknik Digital dan Rangkaian Sekuensial kali ini diberikan sub kasus yang meliputi :

6. Rangkaian sekuensial

6.1 Konsep rangkaian sekuensial
6.2 Rangkaian sekuensial Moore
6.3 Rangkaian sekuensial Mealy
6.4 Finite State Machines (FSM)
6.5 Jenis-jenis Flip-flop (RS, JK, T, dan D)
6.6 Studi kasus rangkaian sekuensial Moore
6.7 Studi kasus rangkaian sekuensial Mealy

Tujuan

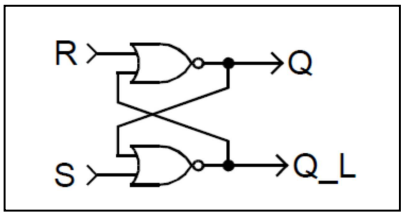
1. Mahasiswa dapat memahami konsep Rangkaian Sekuensial dan Perbedaannya dengan Rangkaian Kombinasional
2. Mahasiswa dapat membedakan antara rangkaian sekuensial Moore dengan Mealy
3. Mahasiswa dapat mengimplementasikan minimasi Fungsi Boolean pada kasus-kasus tertentu sesuai dengan fungsi dan perangkat/komponen yang digunakan
4. Mahasiswa dapat membaca dan merancang rangkaian kombinasional sesuai *requirenment* yang ditentukan

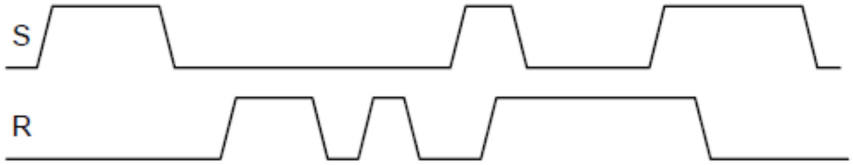
Penilaian

1. Rencana kerja tim
2. Komunikasi dan Diskusi yang dibangun
3. Ketepatan waktu pengerjaan
4. Kebenaran hasil pengerjaan kasus

1. Given SR latch truth table and the Input waveforms shown in figure below, sketch the output, Q, of an SR latch

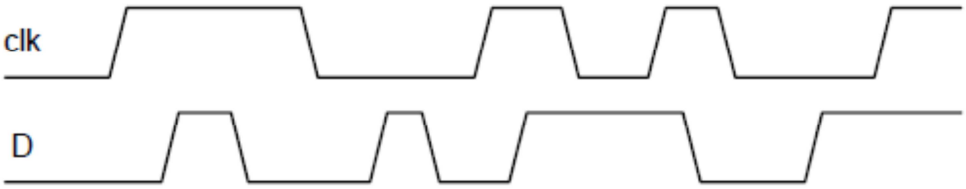
Case	S	R	Q	$\overline{Q}$
IV	0	0	Q_{prev}	$\bar{Q}_{prev}$
I	0	1	0	1
II	1	0	1	0
III	1	1	0	0





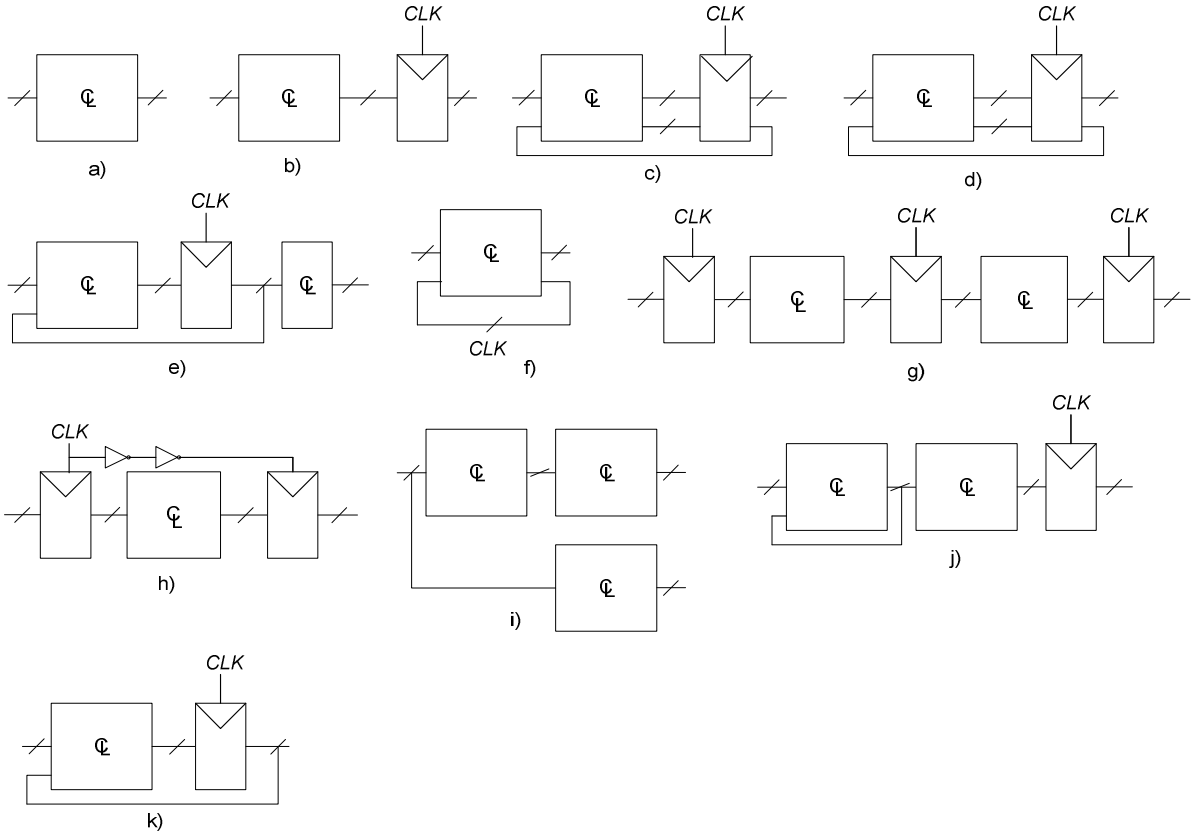
2. Given D latch and D Flip-flop truth table and the Input waveforms shown in figure below, sketch the output, Q, of an D latch and D Flip-flop

CLK	D	$\overline{D}$	S	R	Q	$\overline{Q}$
0	X	$\bar{X}$	0	0	Q_{prev}	$\bar{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0

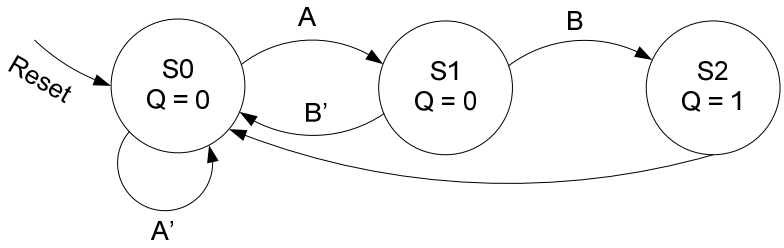


3. A *JK flip-flop* receives a clock and two inputs, *J and* K. On the rising edge of the clock, it updates the output, *Q*. if only *J* and *K* are both 0, *Q* retains its old value. If only *J* is 1, *Q* becomes 1. If only *K* is 1, *Q* becomes 0. If both *J* and *K* are 1, *Q* becomes the opposite of its present state.
   a. Construct a JK flip-flop using a D flip-flop and some combinational logic
   b. Construct a D flip-flop using a JK flip-flop and some combinational logic
   c. Construct a T flip-flop using a JK flip-flop

4. Consider circuits above, which of the circuit in figure above are sychronous sequential circuits ? Explain !



5. Describe in words what the state machine in figure below does. Using binary state encodings, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a shematic of the FSM.



6. Consider the following case. Football players are hustling between the athletic fields and the dining hall on Telecomunication Boulevard. They are tossing the ball back and forth and aren't looking where they are going either. Several serious injuries have already occurred at the intersection of these two roads, and the Dean of Students asks you and your team to install a traffic light before there are fatalities. You and your team, decides to solve the problem with an FSM. You and your team install two traffic sensors, T_A and T_B, on Academic Ave, and Telecomunication Blvd., respectively. Each sensor indicates TRUE if students are present and FALSE if the street is empty. You and your team also decide to installs two traffic light, L_A and L_B, to control traffic. Each light receives digital inputs specifying whether it should be green, yellow, and red. Hence, your FSM has two inputs, T_A and T_B, and two outputs, L_A and L_B. The intersection with lights and sensors is shown in Figure below. You and your team provides a clock with a 5-second period. On each clock tick (rising edge), the light may change based on the traffic sensors. You and your team also provide a reset button so that Physical Plant technicians can put the controller in a knowns initial state when they turn ini on.

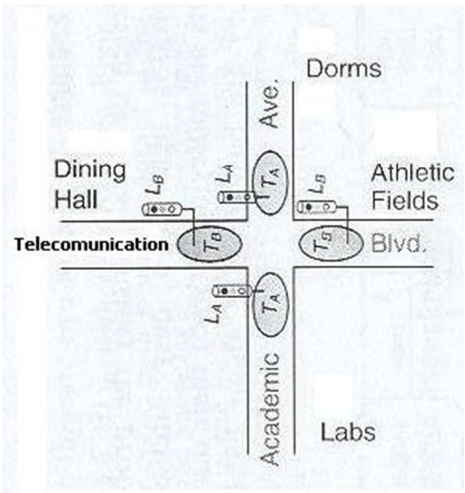
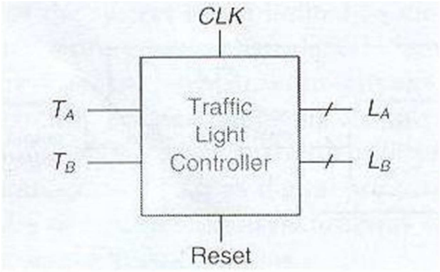


Figure below shows a black box view of the state machine.



When the system is reset, the light are green on Academic Ave, and red on Telecomunication Blvd. Every 5 seconds, the controller examines the traffic pattern and decides what to do next. As long as traffic is present on Academic Ave., the light do not change. When there is no longer traffic on Academic Ave., the light on Academic Ave. becomes yellow for 5 seconds before it turns red and Telecomunication Blvd.'s light turns green. Similarly, the Telecomunication Blvd. light remains green as long as traffic is present on the boulevard, then turns yellow and eventually red.

a. Sketch the *state transition diagram* to indicate all the possible states of the system and the transitions between these states
b. Write the state transition diagram as a state transition table, which indicates, for each state and input, what the next state, *S'*, should be. Note that the table uses don't care symbols (X) whenever the next state does not depend on a particular input. Also note that Reset is omitted from the table. Instead, use resettable Flip-flop that always go to state S0 on reset, independent of the inputs. Use State encoding given in table below.

Table 1. State Encoding

State	Encoding $S_{1:0}$
S0	00
S1	01
S2	10
S3	11

Table 2. Output Encoding

Output	**Encoding $L_{1:0}$**
Green	00
Yellow	01
Red	10

c. Draw your state machine circuit for traffic light controller using Moore FSM form

7. N-FF, LN-FF, GM, and SF-FF has the following operation table :

N	Q_{t+1}
0	$\bar{Q}_t$
1	1

a)

L	N	Q_{t+1}
0	0	1
0	1	Q_t
1	0	$\bar{Q}_t$
1	1	0

b)

G	M	Q_{t+1}
0	0	1
0	1	1
1	0	0
1	1	$\bar{Q}_t$

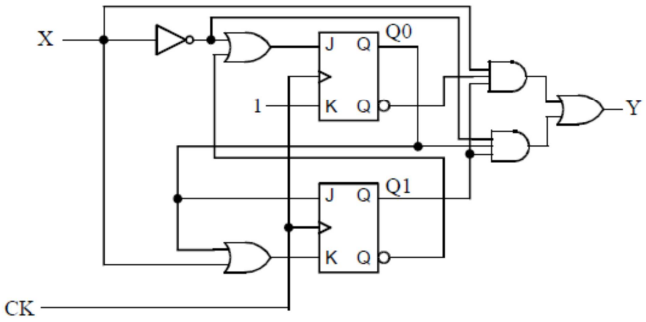
c)

S	F	Q_{t+1}
0	0	1
0	1	$\bar{Q}_t$
1	0	0
1	1	1

d)

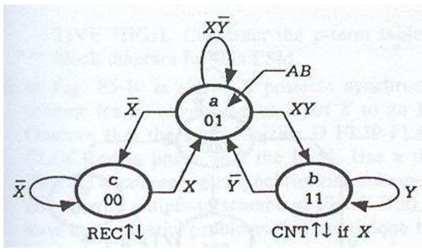
i. Construct the state diagram and state trasition table for all FF above
ii. Construct all FF above using a D-FF and some combinational logic
iii. Construct for all FF above using a JK-FF and some combinational logic

8. Given a sequential circuit below,

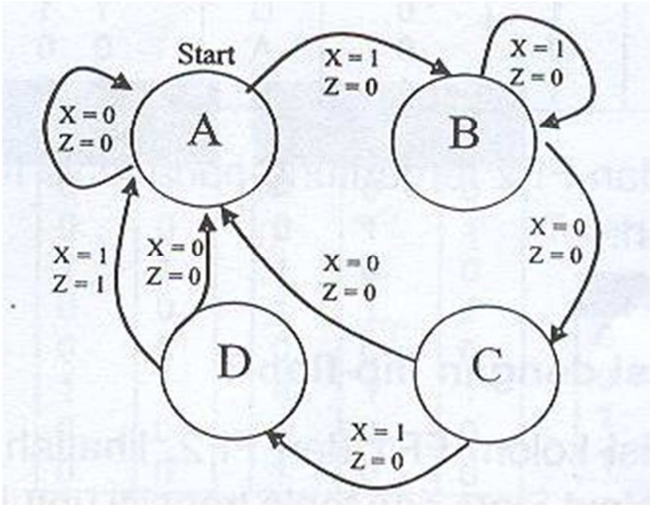


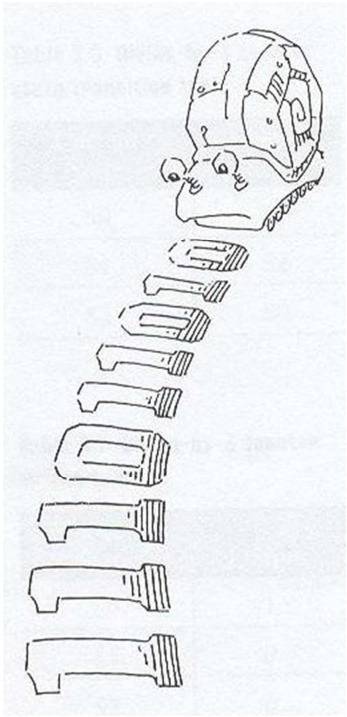
   a. Derive the excitation and output equations
   b. Derive the transition equations from the excitation equations
   c. Construct the transition table from the transition equations

9. Use D-FF and NAND logics to design a logic circuit for the FSM represented by the state diagram in figure below. Assume that all inputs and outputs are ACTIVE HIGH and that triggering occurs on the rising edge of the CLOCK waveform.



10. Make a state table for the following state diagram using the D-FF-FF and JK then implement!





11. Jordan Samsons Owns a pet robotic snail with an FSM brain. The snail crawls from left to right along a paper tape containing a sequence of 1's and 0's. On each clock cycle, the snail crawls to the next bit. The snails smiles when the last four bits that it has crawled over are, from left to right, 1101. Design the FSM to compute when the snail should smile. The input *A* is the bit underneath the snail's antennae. The output Y is TRUE when the snail smiles.
    a. Design Moore and Mealy state machine a pet robotic snail
    b. Write the state transition diagram as a state transition table, which indicates, for each state and input, what the next state, *S'*, should be.